PATENT
Docket No.: 29284/599

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS	:	H. MIZUNO, et al.
SERIAL NO.	:	(Con. of 10/024,039)
FILED	:	(Herewith)
FOR	:	SEMICONDUCTOR INTEGRATED CIRCUIT APPARATUS
GROUP ART UNIT	:	2814
EXAMINER	:	Quan Tra (Anticipated)

COMMISSIONER FOR PATENTS
P. O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. § 1.97 & § 1.98

S I R:

In conformance with Applicants' duty of disclosure under 37 C.F.R. § 1.56 and § 1.97(b)(1), the references listed on the attached form PTO-1449 are hereby brought to the Examiner's attention.

Since all of the references have already been considered in parent application Serial No. 10/024,039, no copies of the references are required.

It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear in the "references cited" on any patent to issue therefrom.

Respectfully submitted,

Date: 16 July 2003

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FORM PTO-1449
INFORMATION DISCLOSURE STATEMENT BY APPLICANT(S)

Atty Docket No. : 29284/599
Serial No. :
Inventors : H. Mizuno et al.
Filed :
Group Art Unit : 2814
Examiner : Quan Tra (Anticipated)

U.S. PATENT DOCUMENTS

Examiner Initial	Patent Number	Patent Date	Name	Class/ Subclass	Filing Date
_____	5,461,338	10-1995	HIRAYAMA et al.	327/314	
_____	5,557,231	09/07/96	YAMAGUCHI et al.	327/534	
_____	5,610,533	03/11/97	ARIMOTO et al.	326/33	
_____	5,703,522	12-1997	ARIMOTO et al.	327/534	
_____	5,726,562	03-1998	MIZUNO, M.	323/312	
_____	5,818,212	10-1998	MIN et al.	323/314	
_____	5,909,140	06-1999	CHOI	327/534	
_____	6,097,113	08-2000	TERAOKA et al.	307/534	
_____	6,337,593	01-2002	MIZUNO et al.	327/534	

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class/ Subclass	Translation Yes	Translation No
_____	0 773 448	05/14/97	EPO		N/A	
_____	7254685	10/03/95	Japan		ABS.	
_____	10-229165	08/25/98	Japan		ABS.	
_____						
_____						

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial

_____ 1. IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, Nov. 1996, pp. 1770-1779

EXAMINER _____ DATE CONSIDERED _____

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.